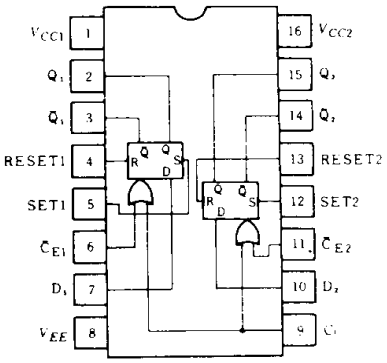
High Speed Dual D-type Master-Slave Flip Flops

The HD10231 is a dual master-slave type D flip-flop. Asynchronous Set(S) and Reset(R) override Clock (C_C) and Clock Enable ($\overline{CE}$) inputs. Each flip-flop may be clocked separately by holding the common clock in the low state and using the enable inputs for the clocking function. If the common clock is to be used to clock the flip-flop, the Clock Enable inputs must be in the low state. In this case, the enable inputs perform the function of controlling the common clock.
The output states of the flip-flop change on the positive transition of the clock. A change in the information present at the data(D) input will not affect the output information at any other time due to master-slave construction.

■PIN ARRANGEMENT



(Top View)

■FUNCTION TABLE

● R-S

R	S	Q_{n+1}	$\overline{Q}_{n+1}$
L	L	Q_n	$\overline{Q}_n$
L	H	H	L
H	L	L	H
H	H	×	×

× : Don't Care

● CLOCK

C	D	Q_{n+1}
L	×	Q_n
↑	L	L
↑	H	H

1. × : Don't Care
2. C = $\overline{C}_E + C_C$
3. ↑ : transition from low to high

■DC CHARACTERISTICS ($V_{EE} = -5.2V$, $Ta = -30 \sim +85°C$)

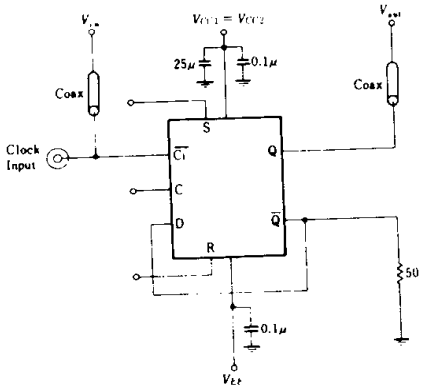
Item	Symbol	Test Condition			min	typ	max	Unit
Supply Current	I_{EE}			25°C	—	52	65	mA
Input Current	I_{IH}	$V_{IH} = -0.810V$	D, $\overline{C_E}$	25°C	—	—	220	μA
			C_C		—	—	290	
			S, R		—	—	410	
	I_{IL}	$V_{IL} = -1.850V$		25°C	0.5	—	—	μA
Output Voltage	V_{OH}	$V_{IH} = -0.890V$ or $V_{IL} = -1.890V$		−30°C	−1.060	—	−0.890	V
		$V_{IH} = -0.810V$ or $V_{IL} = -1.850V$		25°C	−0.960	—	−0.810	
		$V_{IH} = -0.700V$ or $V_{IL} = -1.825V$		85°C	−0.890	—	−0.700	
	V_{OL}	$V_{IL} = -1.890V$ or $V_{IH} = -0.890V$		−30°C	−1.890	—	−1.675	V
		$V_{IL} = -1.850V$ or $V_{IH} = -0.810V$		25°C	−1.850	—	−1.650	
		$V_{IL} = -1.825V$ or $V_{IH} = -0.700V$		85°C	−1.825	—	−1.615	
Output Threshold Voltage	V_{OHA}	$V_{IHA} = -1.205V$ or $V_{ILA} = -1.500V$		−30°C	−1.080	—	—	V
		$V_{IHA} = -1.105V$ or $V_{ILA} = -1.475V$		25°C	−0.980	—	—	
		$V_{IHA} = -1.035V$ or $V_{ILA} = -1.440V$		85°C	−0.910	—	—	
	V_{OLA}	$V_{ILA} = -1.500V$ or $V_{IHA} = -1.205V$		−30°C	—	—	−1.655	V
		$V_{ILA} = -1.475V$ or $V_{IHA} = -1.105V$		25°C	—	—	−1.630	
		$V_{ILA} = -1.440V$ or $V_{IHA} = -1.035V$		85°C	—	—	−1.595	

■ AC CHARACTERISTICS (V_{EE} = −3.2V, V_{CC} = +2.0V, Ta = −30 ~ +85°C)

Item	Symbol	Input	Output	Test Condition		min	typ	max	Unit
Propagation Delay Time	t_{PLH}	$\overline{C}$, $\overline{C}_E$	Q, $\overline{Q}$	R_L = 50Ω,	−30°C	1.4	—	3.4	ns
					25°C	1.5	—	3.3	
					85°C	1.5	—	3.7	
	t_{PHL}				−30°C	1.4	—	3.4	
					25°C	1.5	—	3.3	
					85°C	1.5	—	3.7	
	t_{PLH}	S	Q, $\overline{Q}$		−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
	t_{PHL}				−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
	t_{PLH}	R	Q, $\overline{Q}$		−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
	t_{PHL}				−30°C	1.0	—	3.4	
					25°C	1.1	—	3.3	
					85°C	1.1	—	3.7	
Rise Time	t_{TLH}		Q, $\overline{Q}$		−30°C	0.9	—	3.3	ns
					25°C	1.0	—	3.1	
					85°C	1.0	—	3.5	
Fall Time	t_{THL}				−30°C	0.9	—	3.3	ns
					25°C	1.0	—	3.1	
					85°C	1.0	—	3.5	
Setup Time	t_{su}	D → $\overline{C}$	Q, $\overline{Q}$		25°C	—	—	1.0	ns
Hold Time	t_h				25°C	—	—	0.75	ns
Max. Toggle Frequency	f_{Tog}	—	—		−30°C	200	—	—	MHz
					25°C	200	250	—	
					85°C	200	—	—	

■ TEST CIRCUIT OF AC CHARACTERISTICS

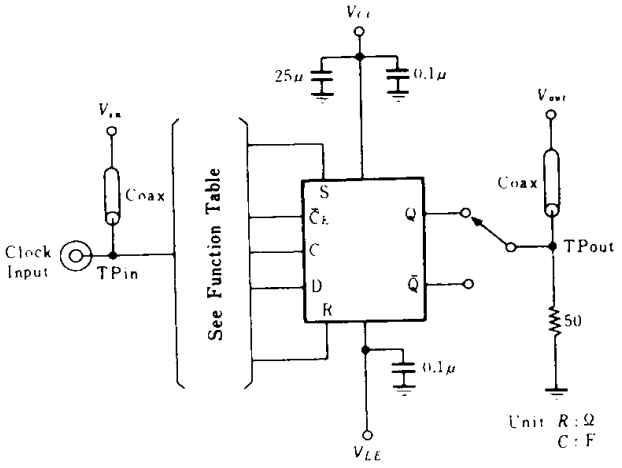
1. Toggle Frequency

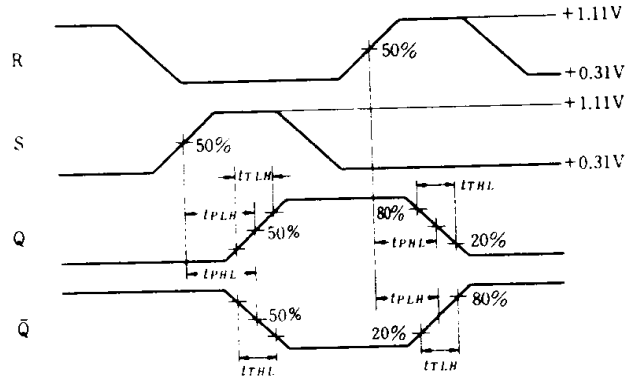


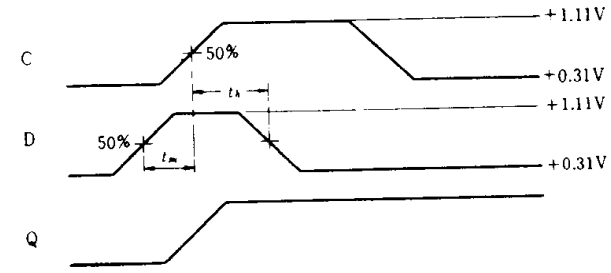
Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.

HITACHI

2. Switching Time







Notes)
1. 50Ω termination to ground located in each scope channel input. All input and output cables to the scope are equal lengths of 50Ω coaxial cable.
2. Wire length should be <6.35mm (1/4 inch) from TPin to input pin and TPout to output pin.
3. t_{su} is the minimum time before the positive transition of the clock pulse that information must be present at the data.
4. t_h is the minimum time after the positive transition of the clock pulse that information must remain unchanged at data.
5. Input Pulse; $t_{TLH}=t_{THL}=1.5\pm0.2$ns (20% to 80%).